Amendment to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Currently amended) A method comprising:

storing a plurality of ~~an~~ instructions in at least two prefetch buffers, each having an associated ~~and a~~ multiple bit exception status information word, the state of bits of the ~~said multiple bit~~ exception words representing multiple different kinds of exceptions, wherein an instruction and the associated exception word may be spread across more than one prefetch buffer;

obtaining each instruction and the associated exception word from the at least two prefetch buffers;

aligning the obtained instructions using the obtained associated exception word;

~~using said exception word to align an instruction associated with said exception status word~~; and

issuing at least part of an aligned instruction and at least part of the exception status word in parallel.

2. (Previously presented) The method of Claim 1, further comprising:

detecting a width of the instruction prior to said issuing the instruction and at least part of the exception status information in parallel.

3. (Previously presented) The method of Claim 1, wherein said issuing the instruction and at least part of exception status information in parallel comprises:

sending the instruction to a decoder; and

sending the exception status information through an OR gate to exception handling logic.

4. (Previously presented) The method of Claim 1, further comprising:

fetching at least one data block;

generating exception status information about an instruction within the data block;

storing the exception status information with the data block; and

detecting at least part of an instruction within the data block.

5. (Original) The method of Claim 4, wherein generating exception status information includes generating information identifying that a particular exception condition was detected.

6. (Original) The method of Claim 4, wherein generating exception status information comprises generating information indicating that a particular exception condition was not detected.

7. (Original) The method of Claim 4, further comprising:

if only part of the instruction is in the data block, fetching another data block containing the rest of the instruction prior to issuing the instruction.

8. (Previously presented) The method of Claim 7, wherein said storing the exception status information represents storing the whole instruction in the multiple data blocks.

9-16. (Canceled)

17. (Currently amended) A system comprising:

a static random access memory device; and

a processor coupled to the memory device, wherein the processor includes an execution unit and a control unit, the control unit including a prefetch unit having at least two prefetch buffers and exception handling logic, the control unit adapted operates to:

fetch at least two ~~one~~ data blocks associated with a single instruction;

generate exception status information for each of ~~about~~ the data blocks, the exception status information being a multiple bit exception status information word, the state of said multiple bit exception word representing multiple different kinds of exceptions;

store the exception status information and the data blocks in the prefetch unit in at least two of the prefetch buffers;

detect at least part of an instruction within the data block;

align said at least part of said instruction, based on said exception status information; and

in parallel, issue the instruction to the execution unit and issue at least part of the exception status information to the exception handling logic.

18. (Original) The system of Claim 17, wherein the control unit is further adapted to:

fetch another data block;

generate additional exception status information about the another data block; and

store the additional exception status information and the another data block in the prefetch unit.

19. (Canceled).

20. (Original) The system of Claim 17, wherein issuing the instruction and at least part of exception status information in parallel comprises:

sending the instruction to the decoder; and

sending the exception status information through an OR gate to the exception handling logic.

21. (New) The system of Claim 17, wherein the exception status information for a particular instruction may include information describing the exception status of at least two data blocks.